65. (New) The device according to claim 63, wherein the floating gate of the selection gate transistor is electrically connected to the control gate of each of the selection gate transistor.

66. (New) The device according to claim 45, wherein the second transistor includes an erasable and programmable memory cell transistor.

C2 cont'd

67. (New) The device according to claim 66, wherein a gate electrode of the erasable and programmable memory cell transistor is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

68. (New) The device according to claim 67, wherein the metal contains tungsten.

IN THE ABSTRACT

**Please replace the Abstract on page 38, with the following paragraph:**[2]

C3

A nonvolatile semiconductor memory device includes a first element region provided in a peripheral circuit region of a semiconductor substrate; a second element region provided in a memory cell region of the substrate; a first element isolation region provided in the substrate; a second element isolation region provided in the substrate; a first transistor having source and drain diffusion layers each provided in the first element region; a second transistor having source and drain diffusion layers each provided in the second element region; and an insulating film covering the first and second transistors. The insulating film is harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film is oxidized.

[2]A marked-up copy of the amended portion of the Abstract is attached hereto.